

Chassis TV-VCR 2004 – 21" Range (Z12VA)

**Main Schematic Diagram
H.V./Power Schematic Diagram
CRT Schematic Diagram
Text Schematic Diagram
Wiring Diagram
Waveforms**

3143 025 22151

Modification 0

Subject to Modification

Sheet 3 of 3

Main 4/5 Schematic Diagram

•

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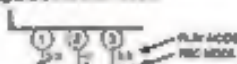
- A. PREPARE CHANNELS TO BE CONNECTED (ANALOGUE) AND REVERSE (7)
- B. PREPARE CHANNELS TO BE WIRE-BOLDED HOLES OF THE PCB (HOLE IS BOLDED) DIRECTLY

STATE POINT INFORMATION

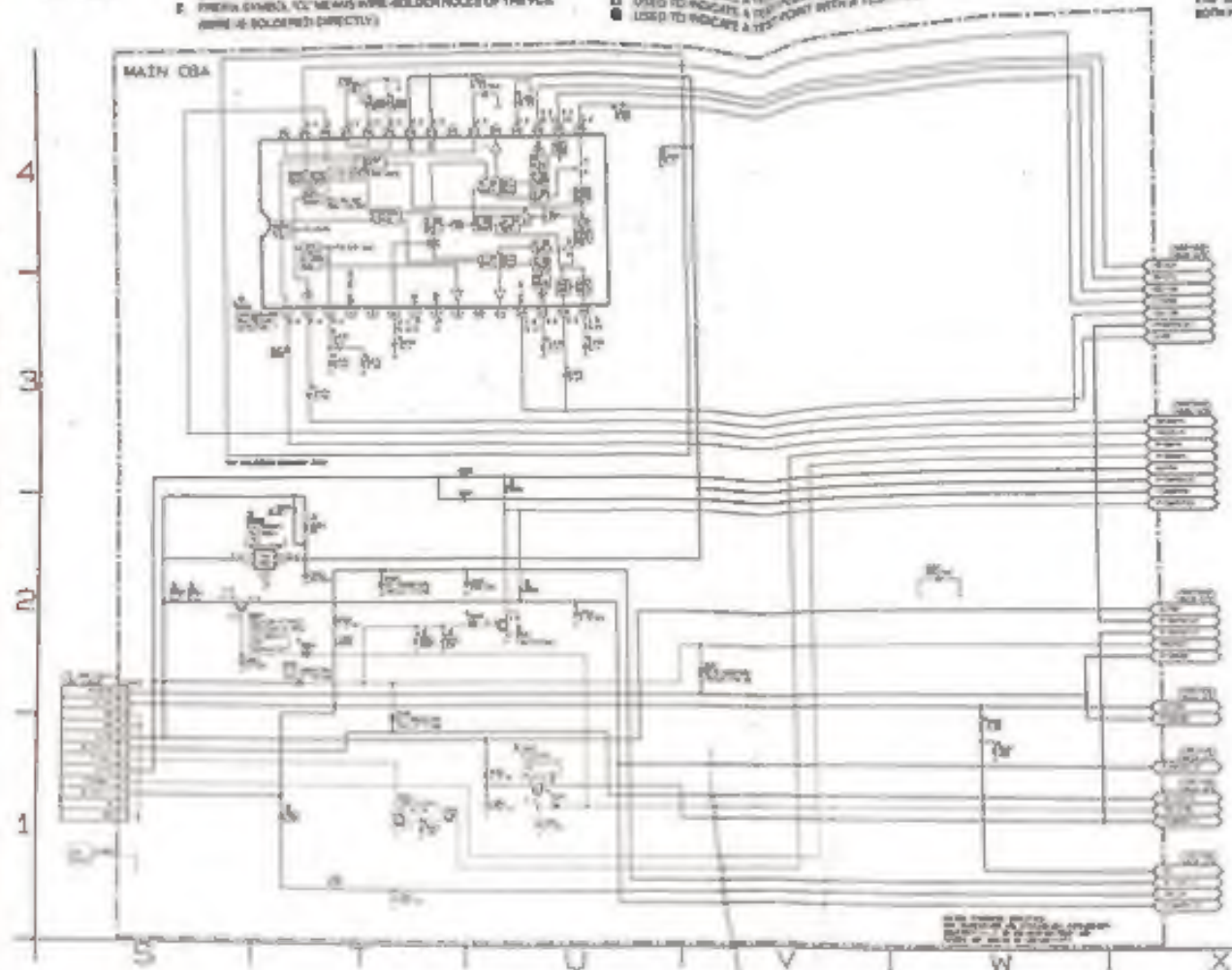
TEST POINT INFORMATION

- INDICATES A TEST POINT WITH A JUMPER WIRE ACROSS A HOLE IN THE PCB
- USED TO INDICATE A TEST POINT WITH A COMPROMISE LEAD ON FOL SIDE
- USED TO INDICATE A TEST POINT WITH NO TEST PIN
- USED TO INDICATE A TEST POINT WITH A TEST PIN

Upgrades including the FLAT and REC added on the Economy Chassis are an almost instant



Find NAME, PHONE, FAX, ADDRESS from the yellow pages under a ABC LETTER. Also listed: Street map.



100% Satisfaction Guarantee

Area	1990	1995	2000
Wages	2.2	5	1.9
Profits	0	0	0
Costs	8	7.9	8
Output	0.3	0	0
Capital	1	2.6	0
Labour	0	4.7	0

Table 1

Intensity (photons/μm ² /s)	Exposure (s)	Age (yr)	Region
100	100	0.250	1
100	100	0.250	2
100	100	0.250	3
100	100	0.250	4
100	100	0.250	5
100	100	0.250	6
100	100	0.250	7
100	100	0.250	8
100	100	0.250	9
100	100	0.250	10
100	100	0.250	11
100	100	0.250	12
100	100	0.250	13
100	100	0.250	14
100	100	0.250	15
100	100	0.250	16
100	100	0.250	17
100	100	0.250	18
100	100	0.250	19
100	100	0.250	20
100	100	0.250	21
100	100	0.250	22
100	100	0.250	23
100	100	0.250	24
100	100	0.250	25
100	100	0.250	26
100	100	0.250	27
100	100	0.250	28
100	100	0.250	29
100	100	0.250	30
100	100	0.250	31
100	100	0.250	32
100	100	0.250	33
100	100	0.250	34
100	100	0.250	35
100	100	0.250	36
100	100	0.250	37
100	100	0.250	38
100	100	0.250	39
100	100	0.250	40
100	100	0.250	41
100	100	0.250	42
100	100	0.250	43
100	100	0.250	44
100	100	0.250	45
100	100	0.250	46
100	100	0.250	47
100	100	0.250	48
100	100	0.250	49
100	100	0.250	50
100	100	0.250	51
100	100	0.250	52
100	100	0.250	53
100	100	0.250	54
100	100	0.250	55
100	100	0.250	56
100	100	0.250	57
100	100	0.250	58
100	100	0.250	59
100	100	0.250	60
100	100	0.250	61
100	100	0.250	62
100	100	0.250	63
100	100	0.250	64
100	100	0.250	65
100	100	0.250	66
100	100	0.250	67
100	100	0.250	68
100	100	0.250	69
100	100	0.250	70
100	100	0.250	71
100	100	0.250	72
100	100	0.250	73
100	100	0.250	74
100	100	0.250	75
100	100	0.250	76
100	100	0.250	77
100	100	0.250	78
100	100	0.250	79
100	100	0.250	80
100	100	0.250	81
100	100	0.250	82
100	100	0.250	83
100	100	0.250	84
100	100	0.250	85
100	100	0.250	86
100	100	0.250	87
100	100	0.250	88
100	100	0.250	89
100	100	0.250	90
100	100	0.250	91
100	100	0.250	92
100	100	0.250	93
100	100	0.250	94
100	100	0.250	95
100	100	0.250	96
100	100	0.250	97
100	100	0.250	98
100	100	0.250	99
100	100	0.250	100

H.V./Power Supply 1/2 Schematic Diagram

CAUTION

CAUTION Fixed voltage (or Auto voltage selectable) power supply circuit is used in this unit. If Main Fuse (F80T) is blown, check to see that all components in the power supply circuit are not defective before you connect the AC plug to the AC power supply. Otherwise it may cause some components in the power supply circuit to fail.

CAUTION

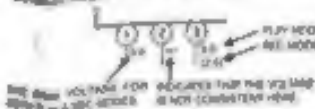
CAUTION
FOR CONTINUED PROTECTION AGAINST FIRE HAZARD,
REPLACE FUSE IMMEDIATELY.

REPLACE ONLY WITH THE SAME TYPE FUSE.

NOTE

NOTE
The voltage for parts in hot circuit is measured using hot GND as a common terminal.

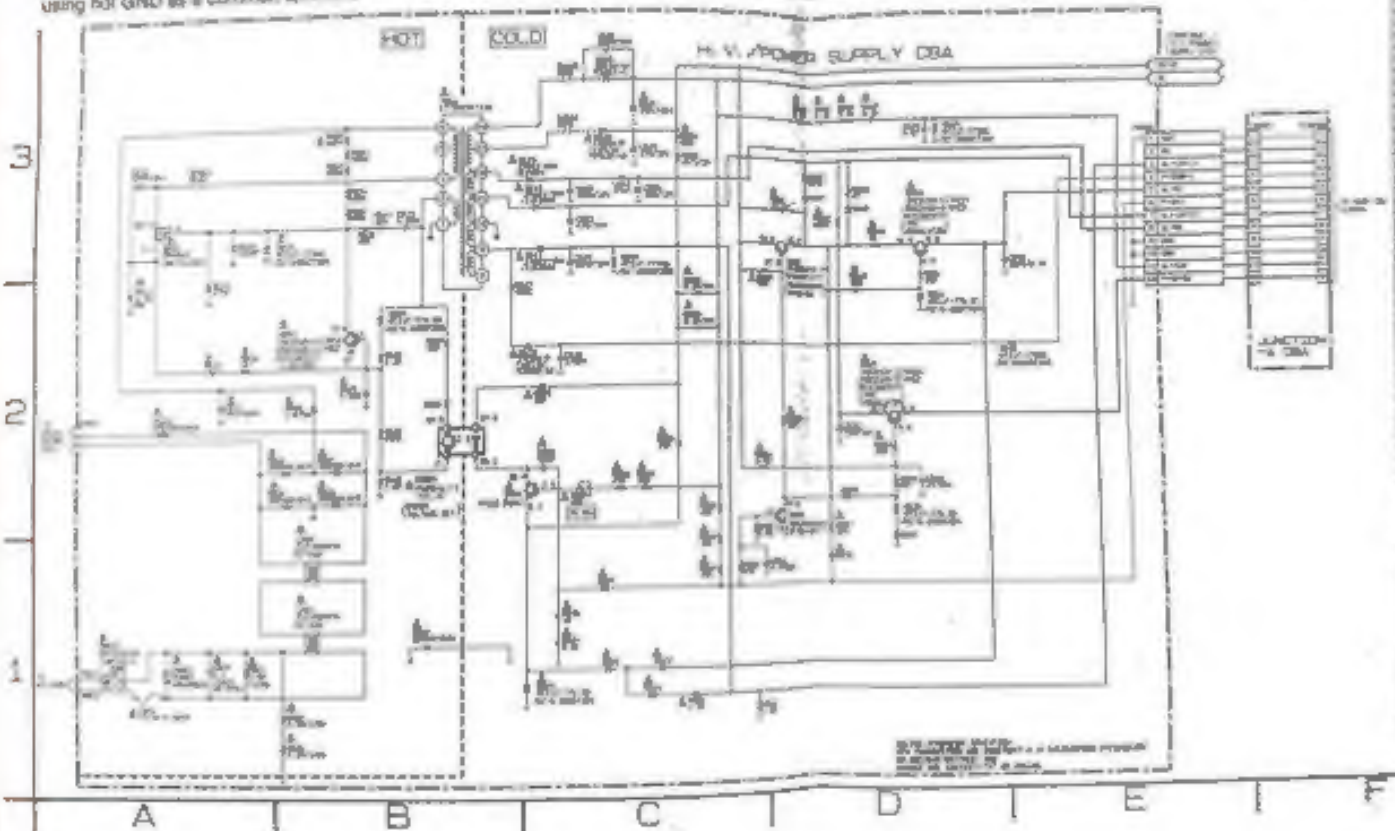
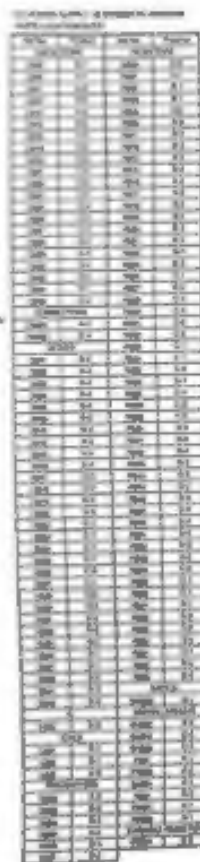
Wichtig: Informieren Sie Ihren Arzt, wenn Sie eine dieser Beschwerden haben:



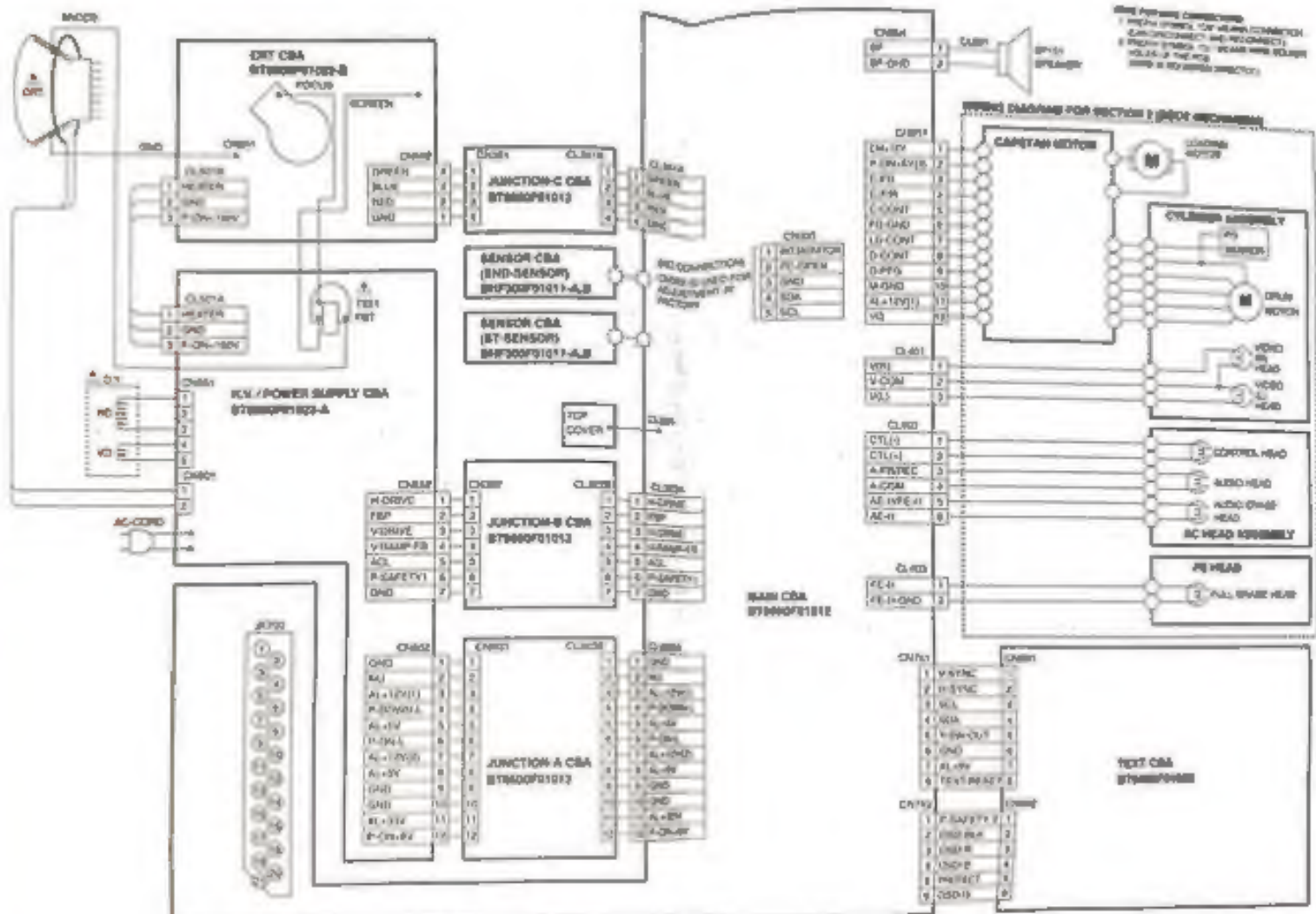
MAPTE: From today onwards

1. HEATS (HUBS) MEANS CONNECTOR (CAN DISCONNECT AND RECONNECT)
2. HEATS (HUBS) MEANS WIRE-SOLDER HOLES OF THE PCB (WIRE IS SOLDERING CONTACT)

FOR FURTHER DETAILS PLEASE SEE LISTING

[illegible]

Wiring Diagram

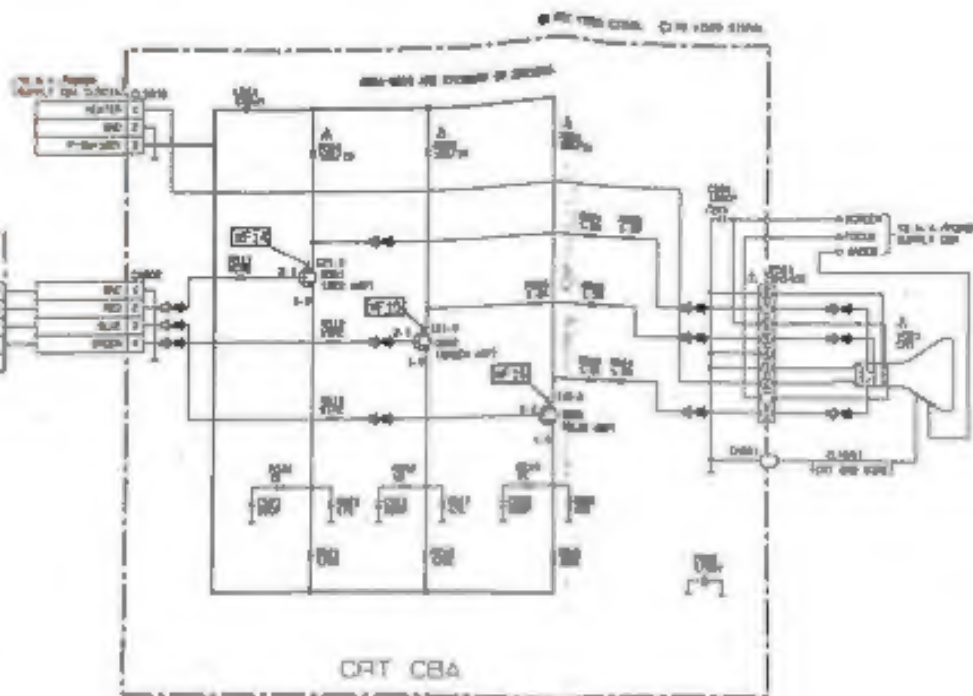
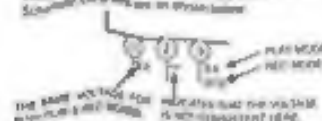


CRT Schematic Diagram

NOTE FOR WIRE CONNECTORS

1. PHOTO SYMBOLS (ON MEANS CONNECTOR (ON MEANS MEANS) AND (ON MEANS MEANS))
2. PHOTO SYMBOLS (ON MEANS MEANS) AND (ON MEANS MEANS)
3. PHOTO SYMBOLS (ON MEANS MEANS) AND (ON MEANS MEANS)

Values indicated by (P) and (R) in the Schematic Diagram are in parentheses.



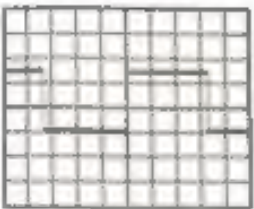
WIRE CONNECTOR (WIRE)

WIRE CONNECTOR (WIRE)

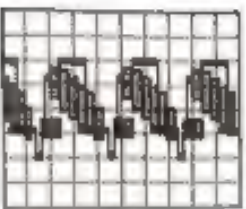
Wire No.	Wire No.
100	100
101	101
102	102
103	103
104	104
105	105
106	106
107	107
108	108
109	109
110	110
111	111
112	112
113	113
114	114
115	115
116	116
117	117
118	118
119	119
120	120
121	121
122	122
123	123
124	124
125	125
126	126
127	127
128	128
129	129
130	130
131	131
132	132
133	133
134	134
135	135
136	136
137	137
138	138
139	139
140	140
141	141
142	142
143	143
144	144
145	145
146	146
147	147
148	148
149	149
150	150
151	151
152	152
153	153
154	154
155	155
156	156
157	157
158	158
159	159
160	160
161	161
162	162
163	163
164	164
165	165
166	166
167	167
168	168
169	169
170	170
171	171
172	172
173	173
174	174
175	175
176	176
177	177
178	178
179	179
180	180
181	181
182	182
183	183
184	184
185	185
186	186
187	187
188	188
189	189
190	190
191	191
192	192
193	193
194	194
195	195
196	196
197	197
198	198
199	199

WAVEFORMS

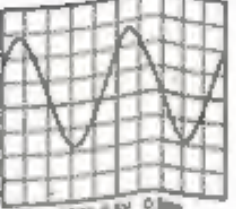
WAVEFORM NOTES
INPUT COLOR BAR SIGNAL
OTHER CONTROLS: CENTER POSITION
VOLTAGES SHOWN ARE RANGE OF
OSCILLOSCOPE SETTING



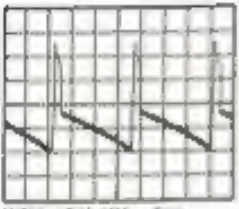
WF1 10DIV 2V 5ms
TP002 RF-SVR



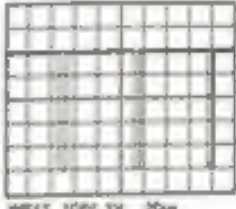
WF5 10DIV 0.5V 20µs
TP003 V-OUT



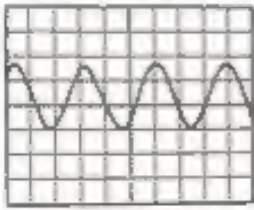
WF9 10DIV 0.5V 0.5ms
IC401 PIN 8



WF13 10DIV 10V 5ms
CN53 PIN 5



WF17 10DIV 1V 20ms
IC201 PIN 5B



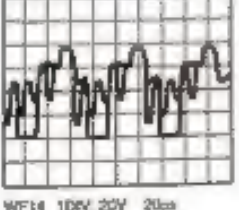
WF2 10DIV 0.2V 0.1µs
IC401 PIN 2B



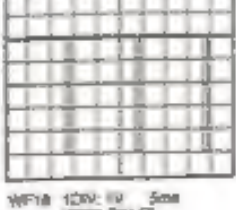
Upper: WF5 Lower: WF1
10DIV 0.2V 20DIV 5V 5ms
TP008 C-FB



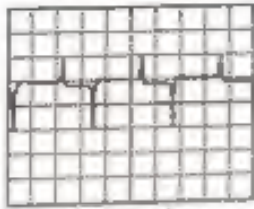
WF10 10DIV 2V 5ms
IC501 PIN 13



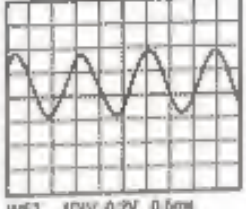
WF14 10DIV 20V 20µs
Q501 COLLECTOR



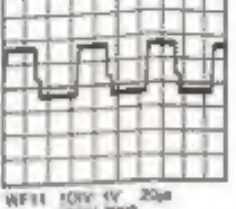
WF18 10DIV 1V 5ms
IC201 PIN 5B



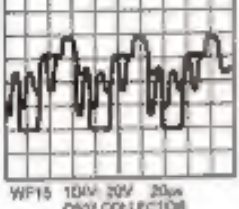
WF3 10DIV 1V 10ms
TP001 C-TL



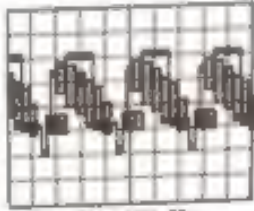
WF7 10DIV 0.2V 0.5ms
IC301 PIN 52



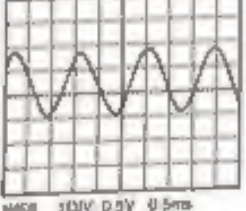
WF11 10DIV 1V 20µs
IC301 PIN 7



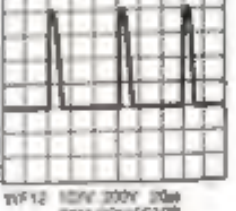
WF15 10DIV 20V 20µs
Q502 COLLECTOR



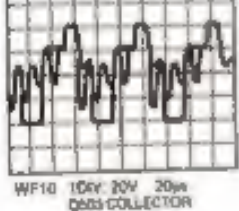
WF4 10DIV 0.25V 20µs
IC401 PIN 4B



WF8 10DIV 0.5V 0.5ms
TP007 N-A-PB



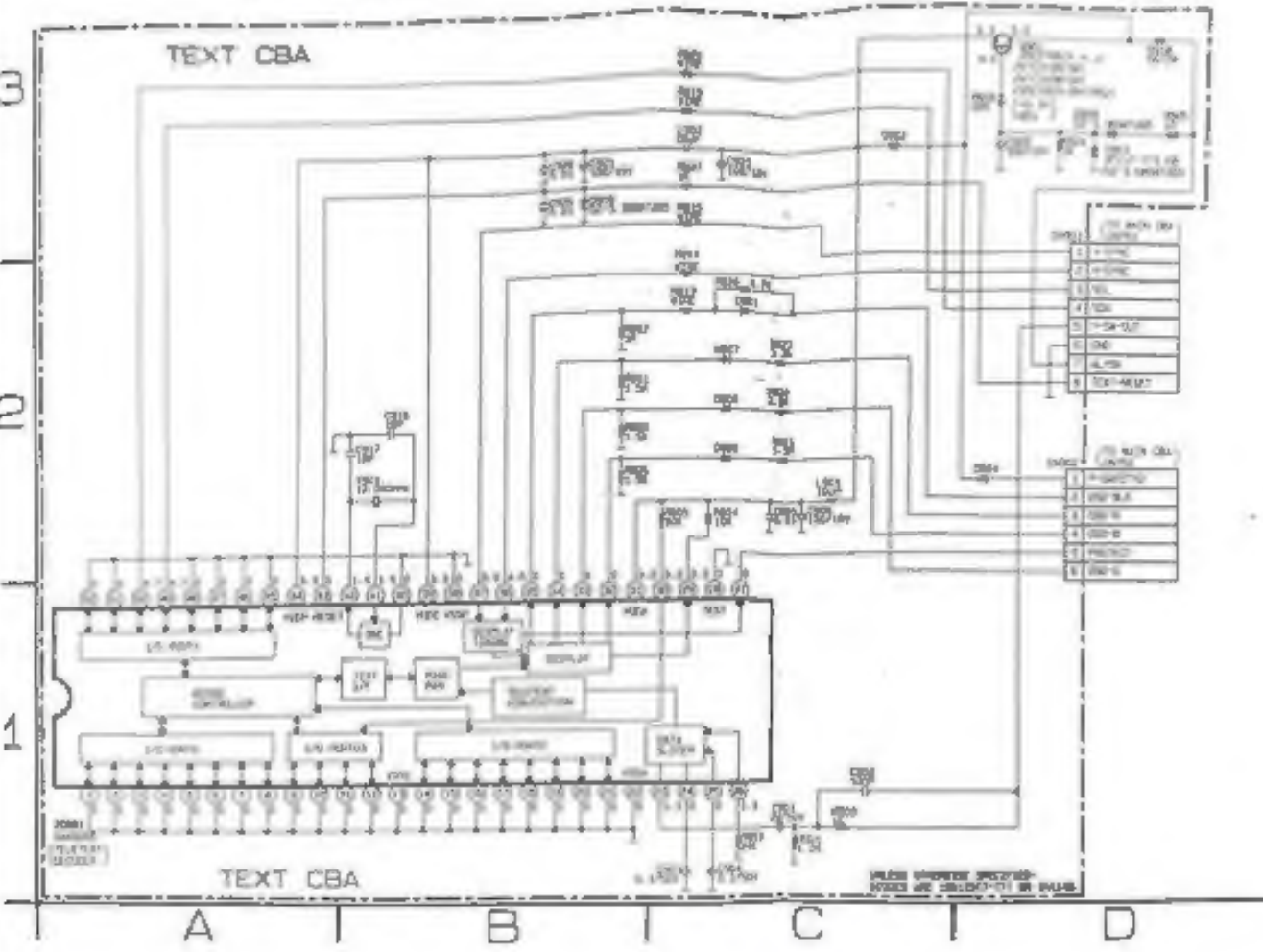
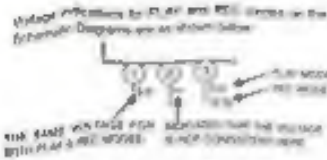
WF12 10DIV 200V 20µs
Q501 COLLECTOR



WF16 10DIV 20V 20µs
Q503 COLLECTOR

Text Schematic Diagram

- NOTE FOR WIRE CONNECTIONS:
- 1. PENDING SYMBOL 'ON' MEANS CONNECTOR (CAN DISCONNECT AND RECONNECT)
 - 2. PENDING SYMBOL 'TV' MEANS WIRE SOLDER HOLES OF THE PCB (NONE IS SOLDERED DIRECTLY)



WIRE CONNECTIONS

WIRE NO.	FROM	TO
1	PL-47	REC
2	PL-47	REC
3	PL-47	REC
4	PL-47	REC
5	PL-47	REC
6	PL-47	REC
7	PL-47	REC
8	PL-47	REC
9	PL-47	REC
10	PL-47	REC
11	PL-47	REC
12	PL-47	REC
13	PL-47	REC
14	PL-47	REC
15	PL-47	REC
16	PL-47	REC
17	PL-47	REC
18	PL-47	REC
19	PL-47	REC
20	PL-47	REC
21	PL-47	REC
22	PL-47	REC
23	PL-47	REC
24	PL-47	REC
25	PL-47	REC
26	PL-47	REC
27	PL-47	REC
28	PL-47	REC
29	PL-47	REC
30	PL-47	REC
31	PL-47	REC
32	PL-47	REC
33	PL-47	REC
34	PL-47	REC
35	PL-47	REC
36	PL-47	REC
37	PL-47	REC
38	PL-47	REC
39	PL-47	REC
40	PL-47	REC
41	PL-47	REC
42	PL-47	REC
43	PL-47	REC
44	PL-47	REC
45	PL-47	REC
46	PL-47	REC
47	PL-47	REC
48	PL-47	REC
49	PL-47	REC
50	PL-47	REC
51	PL-47	REC
52	PL-47	REC
53	PL-47	REC
54	PL-47	REC
55	PL-47	REC
56	PL-47	REC
57	PL-47	REC
58	PL-47	REC
59	PL-47	REC
60	PL-47	REC
61	PL-47	REC
62	PL-47	REC
63	PL-47	REC
64	PL-47	REC
65	PL-47	REC
66	PL-47	REC
67	PL-47	REC
68	PL-47	REC
69	PL-47	REC
70	PL-47	REC
71	PL-47	REC
72	PL-47	REC
73	PL-47	REC
74	PL-47	REC
75	PL-47	REC
76	PL-47	REC
77	PL-47	REC
78	PL-47	REC
79	PL-47	REC
80	PL-47	REC
81	PL-47	REC
82	PL-47	REC
83	PL-47	REC
84	PL-47	REC
85	PL-47	REC
86	PL-47	REC
87	PL-47	REC
88	PL-47	REC
89	PL-47	REC
90	PL-47	REC
91	PL-47	REC
92	PL-47	REC
93	PL-47	REC
94	PL-47	REC
95	PL-47	REC
96	PL-47	REC
97	PL-47	REC
98	PL-47	REC
99	PL-47	REC
100	PL-47	REC

Main 1/5 Schematic Diagram

● = SMD

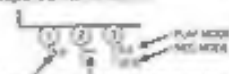
NOTE FOR WIRE CONNECTORS

1. WIRE SYMBOL ON MEANS CONNECTOR (CAN DISCONNECT AND RECONNECT)
2. WIRE SYMBOL ON MEANS ARE SOLDER PINS OF THE PCB (WIRE IS SOLDERED DIRECTLY)

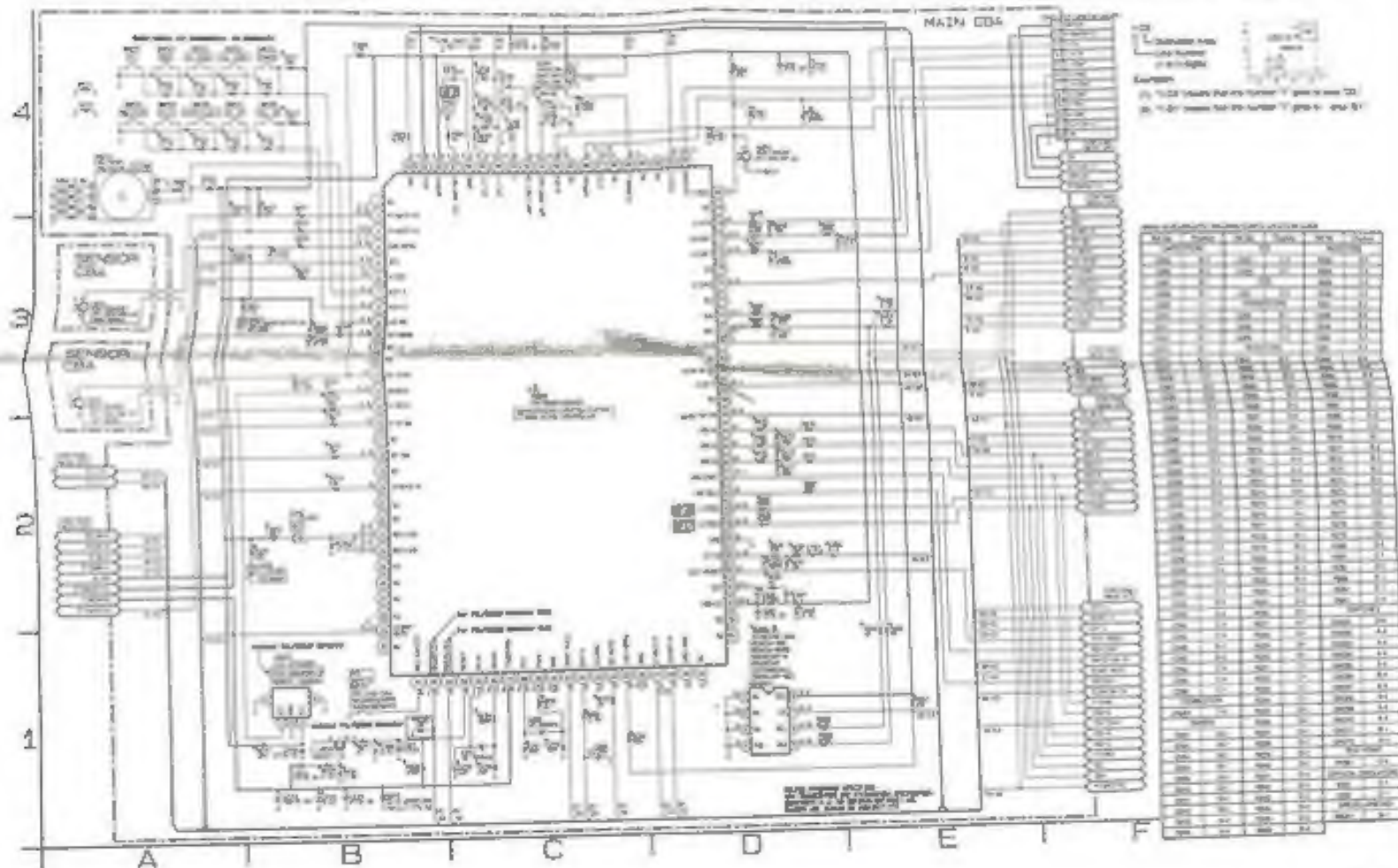
TEST POINT INFORMATION

1. INDICATES A TEST POINT WITH A JUMPER WIRE ACROSS A HOLE IN THE PCB
2. USED TO INDICATE A TEST POINT WITH A COMPONENT LEAD ON PCB SIDE
3. USED TO INDICATE A TEST POINT WITH NO TEST PIN
4. USED TO INDICATE A TEST POINT WITH A TEST PIN

Wedge indicates the PLAT and PCB layers of the Schematic Diagrams are as shown below



THE SAME POSITION FOR PLAT AND PCB LAYERS ARE INDICATED HERE



Main 5/5 Schematic Diagram

••• = GND

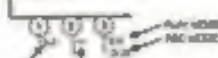
NOTE FOR WIRE CONNECTIONS

1. WIRE SYMBOL "TM" MEANS CONNECTOR (CAN DISCONNECT AND RECONNECT)
2. WIRE SYMBOL "SD" MEANS WIRE BOLDER HOLES UP THE PCB (WIRE IS BOLDED DIRECTLY)

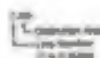
TEST POINT INFORMATION

- INDICATES A TEST POINT WITH A LEADER WIRE ACROSS A HOLE IN THE PCB
- ◐ USED TO INDICATE A TEST POINT WITH A PERMANENT LEAD ON POL. SIDE
- ◑ USED TO INDICATE A TEST POINT WITH NO TEST PIN
- USED TO INDICATE A TEST POINT WITH A TEST PIN

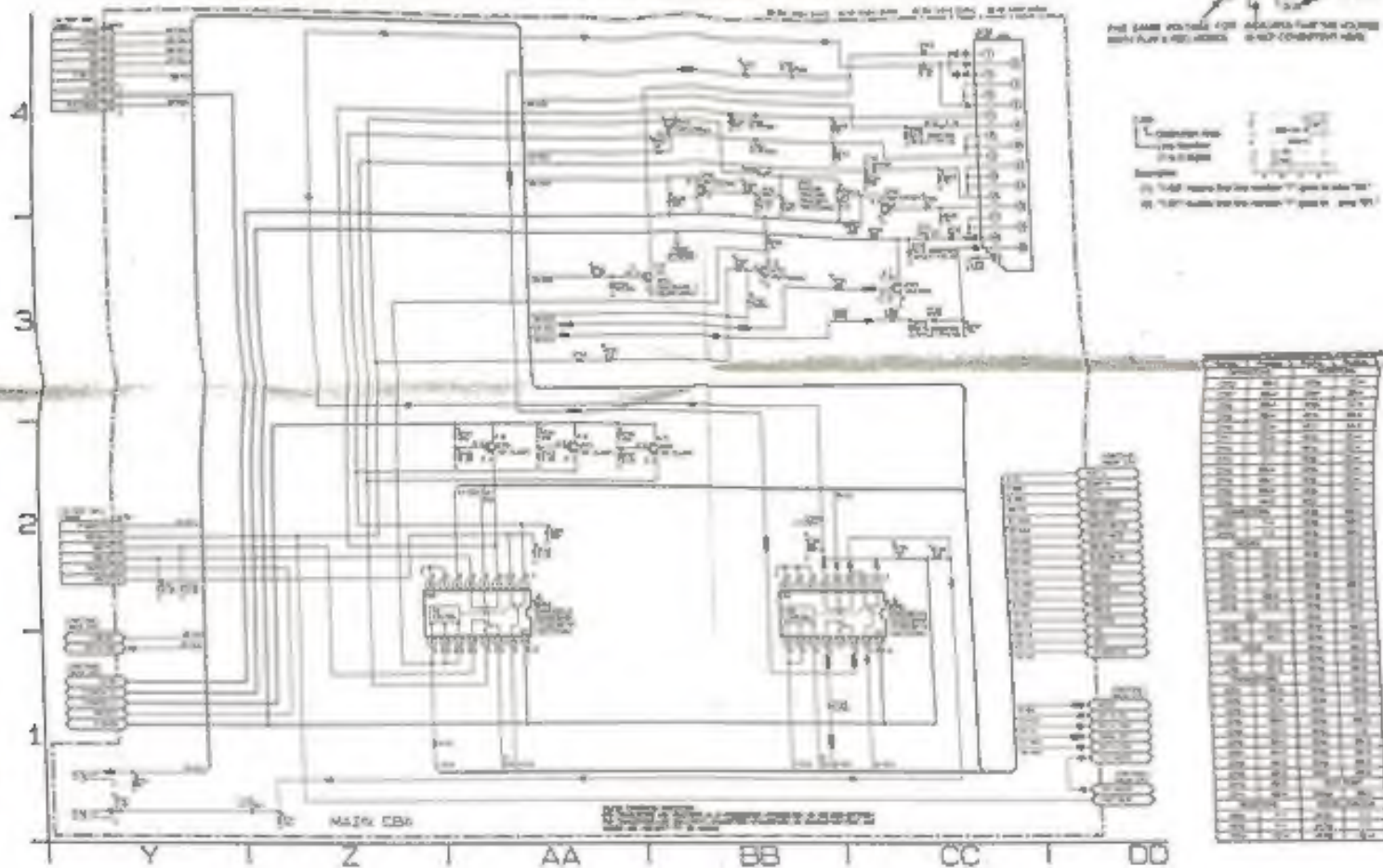
Wiring Addendum for PLM 340 PCB: copies on the topographic diagrams are as shown below



PWR 500M PIN 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67, 68, 69, 70, 71, 72, 73, 74, 75, 76, 77, 78, 79, 80, 81, 82, 83, 84, 85, 86, 87, 88, 89, 90, 91, 92, 93, 94, 95, 96, 97, 98, 99, 100



Examples:
 (1) "100" means the test number "1" goes to hole "100"
 (2) "100" means the test number "1" goes to hole "100"






Main 3/5 Schematic Diagram

$$+ \frac{1}{2} \frac{d^2 \sigma}{d\tau^2} + \frac{1}{6} \frac{d^3 \sigma}{d\tau^3} + \dots$$

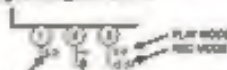
WHERE HAVE WE COME FROM

6. PREPARE WAVE-TO-WAVE CONNECTION (CARDS/CHAINED? AND RECONNECT)
7. PREPARE WAVE-TO-WAVE-BOILER-HOLES OF THE PCB (WAVE-TO-WAVE-BOILER-HOLES)

Abstract

-  INDICATES A TEST POINT WITH A JUMPER WIRE ACROSS A HOLE IN THE PCB
 USED TO INDICATE A TEST POINT WITH A COMPONENT LEAD ON PCB, NOT USED TO INDICATE A TEST POINT WITH NO TEST PIN
 USED TO INDICATE A TEST POINT WITH A TEST PIN

Abbreviations for FLN and PNC resulted in the diagnosis. Diagnosis was as severe as:



THE SAME SYSTEM FOR
THE PLAYERS AND MONITOR

